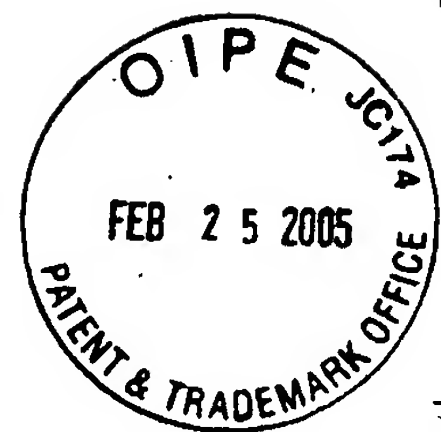


SON-2810

Appl. No. 10/647,217

JPW



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yoshitaka Kayukawa et al.

Confirmation No.: 1901

Application No.: 10/647,217

Art Unit: 2811

Filed: August 26, 2003

Examiner: Violet McCoy

For: SEMICONDUCTOR INTEGRATED CIRCUIT
AND METHOD FOR TESTING SAME

STATUS INQUIRY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is respectfully requested that the attorney named below be advised of the status of the above-identified application. Specifically, please advise us of when an initial Office Action on the merits may be expected from the Patent and Trademark Office. The application has now been pending approximately 18 months without an action on the merits.

Dated: February 25, 2005

Respectfully submitted,

By 

Ronald P. Kananen

Registration No.: 24,104

RADER, FISHMAN & GRAUER PLLC

1233 20th Street, N.W.

Suite 501

Washington, DC 20036

(202) 955-3750

Attorney for Applicant